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Evaluation on Negative Voltage Analysis Model for Gate Driving of MOSFET Application

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Abstract: In power converter or inverter applications, MOSFETs are used as switches to control the value of output current or voltage. The MOSFET turn on/off are controlled by the PWM control IC or MCU with gate driver to achieve high frequency switching. In general, the absolute maximum negative voltage rating of the driving pin at the control IC or gate driver is not sufficient and the driving pin could be damaged by negative voltage which could be induced by the high frequency switching during the MOSFET turn on/off. The main purpose of this paper is to derive and adopt the negative voltage analysis model to evaluate and find out the MOSFET parameter relation which leads to the control IC damaged by negative voltage. The experimental results are demonstrated on the LLC converter with 400 V input voltage and 12 V output voltage. The negative voltage waveforms are measured from the LLC half bridge and synchronous rectifier circuits. Several experimental results are presented to validate this analysis model.

Keywords: Parameters of MOSFET, PWM control IC, Gate driver, Negative voltage, LLC converter.

1. Introduction

In many of switching power supply applications, the gate drive pin of the control IC could be damaged by the negative voltage over the maximum rating. The driving of the power MOSFET is related to the switching speed of the turn-on/off in the switching power supply design [1-3]. The characteristic of the MOSFET and the capability of the gate driver need to be checked at the same time [4- 8]. Due to the parasitic inductance of the MOSFET lead and PCB circuit trace, the driving circuit loop could generated the negative voltage by high current deviation at the reverse recovery time of the MOSFET body diode [9-11]. This paper introduces negative voltage analysis model for gate driving. The next section presents operation principle of gate driving and derivation of analysis model. Experimental results are presented in Section 3 and the conclusion is given in Section 4.

2. Implementation of Circuit

Among circuitry topologies for the switching power supply, LLC converter is chosen for negative voltage measurement and its main DC/DC and synchronous rectifier circuits are shown as Fig. 1. The S_1 and S_2 are the high voltage MOSFETs of half bridge and configured to output the square wave voltage. The low voltage MOSFETs S_3 and S_4 are the power switches of the secondary side synchronous rectifier to minimize power loss.

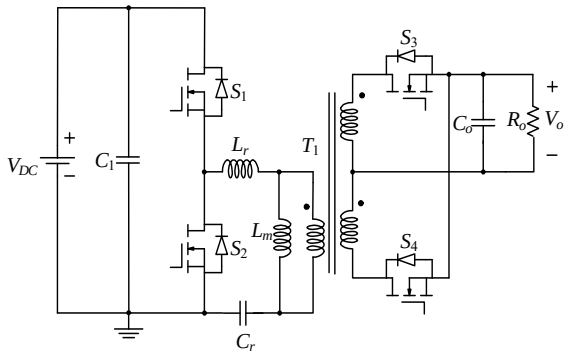

Fig. 1. The LLC converter for application.

2.1. Gate Resistor

The switching speed of the turn-on/off is related the parasitic capacitance of the MOSFET and gate driving circuit [12-14]. The basic driving circuit is shown as Fig. 2. The resistor R_{gs} is to make the gate-source voltage down to zero volts while the gate-source voltage is open. Therefore, we recommend placing 10 kΩ~100 kΩ resistor for reducing malfunction of the switch. The gate resistors R_{g_ext} and R_g and the capacitance C_{iss} would affect the switching speed and the switching loss. For gate resistor selection to reduce switching loss, the following equation is recommended for the setting of gate to source voltage rise/fall time by 5 time constants:

$$t_{rise/fall} = 5 \times (R_{g\_ext} + R_g) \times C_{iss} \ , \quad (1)$$

where C_{iss} is the input capacitance. R_g is the internal gate resistor. R_{g_ext} is the external resistor to change the switching speed for efficiency, thermal or EMI optimization in the gate drive circuit [15, 16]. From Potens' experience, we choose:

$$\frac{t_{period}}{t_{rise/fall}} \geq 50 \ , \quad (2)$$

where t_{period} is the period (cycle duration). The relation of the period and the switching frequency f_s is:

$$t_{period} = \frac{1}{f_s} \quad (3)$$

From equation (1) to (3), R_{g_ext} can be expressed as below:

$$R_{g\_ext} \leq \frac{1}{250 \times f_s \times C_{iss}} - R_g \ , \quad (4)$$

We can use equation (4) to determine the suitable external resistor for the gate drive circuit.

2.2. Negative Voltage Analysis Model

The gate drive circuit loop with parasitic inductance L_{P1}, the gate drive voltage V_{GS}, the gate drive resistor R_g, the gate drive resistor voltage V_R, the gate drive current I_g, and gate to source voltage V_{gs} are shown in Fig. 3.

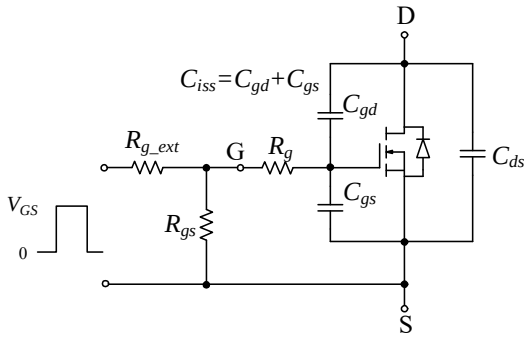

Fig. 2. The basic gate drive circuit.

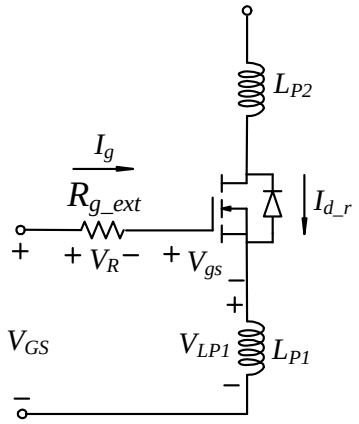

Fig. 3. The gate drive circuit with parasitic inductance.

In reverse recovery related period, I_{d_r} is defined as the current of body diode. Fig. 4 is the relation between the reverse current of body diode and the voltage of parasitic inductance. The I_{RM} is the maximum reverse current of body diode, t_{rr_P} is the period of the positive induced voltage and t_{rr_N} is the period of the negative induced voltage. Therefore, the magnitude of the negative voltage can be derived as

$$V_{LP1} = L_{P1} \times \frac{dI_{d\_r}}{dt} = L_{P1} \times \frac{0 - I_{RM}}{t_{rr\_N}} = -L_{P1} \times \frac{I_{RM}}{t_{rr_N}} \ , \quad (5)$$

The relation of the reverse recovery charge, the reverse recovery time and the maximum reverse current is shown as

$$Q_{rr} = \frac{1}{2} I_{RM} \times t_{rr} \ , \quad (6)$$

The duration of the negative voltage means the energy stress on the gate drive pin of the control IC. The more duration the negative voltage sustains; the more control IC will be damaged. Therefore, we can drive the negative voltage energy as

$$A = |V_{LP1}| \times t_{rr\_N} \tag{7}$$

Substitute equation (5) and (6) into (7), we can derive the area of the negative voltage energy as

$$A = 2 \times L_{P1} \times \frac{Q_{rr}}{t_{rr}} \tag{8}$$

The equation (8) means that the energy might damage the IC is related to the ratio of the reverse recovery charge and the reverse recovery time.

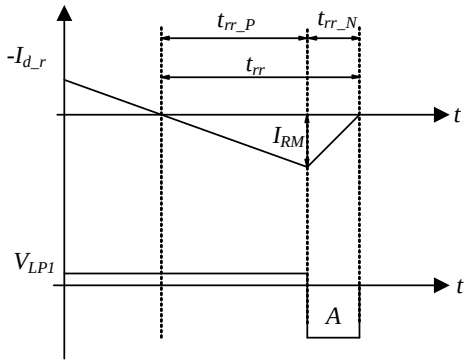

Fig. 4. Relation between Id current and negative voltage.

From the above relation, we can established the negative voltage analysis model considers the influence on the gate drive circuit and MOSFET equivalent circuit. The MOSFET parameters are the inputs of model and the parasitic parameter is measured from circuit loop inductance. By this analysis model, we can obtain the negative voltage as the output and estimate the influence of the negative voltage on the gate drive pin of the control IC from this model. Fig. 5 is the negative voltage analysis model. In gate drive circuit, the gate drive voltage can be derived as

$$\begin{aligned} V_{GS} &= V_{L_{P1}} + V_R + V_{gs} \\ &= L_{P1} \times \frac{dI_{d\_r}}{dt} + V_{gs} + I_g \times R_g \end{aligned} \tag{9}$$

When the gate drive resistor is increased, the magnitude of the negative voltage is decreased shown as the following relationship:

$$R_g \uparrow \Rightarrow |V_{GS}| \downarrow \tag{10}$$

From above relation, the smaller the negative voltage is, the smaller the energy is. Therefore, the possibility of IC damaged is being low by increasing the gate drive resistor.

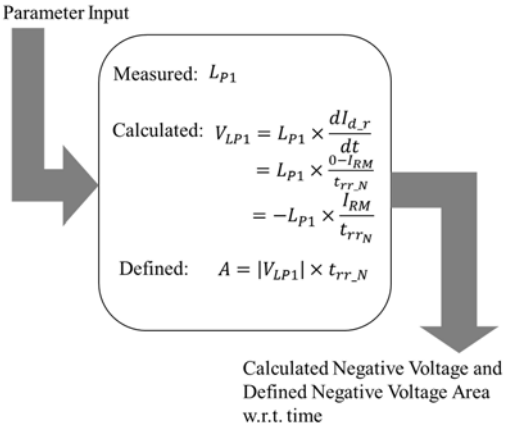

Fig. 5. Negative voltage analysis model.

3. Verification Based on Experimental Result

To demonstrate the effectiveness of the proposed analysis model, a 300 W LLC converter platform is chosen for demonstration. The negative voltage is measured and verified through this LLC converter platform with primary side half bridge and secondary side synchronous rectifier. Fig. 6 is the LLC circuit evaluation board and its main component selection and circuit parameters are given in Table 1.

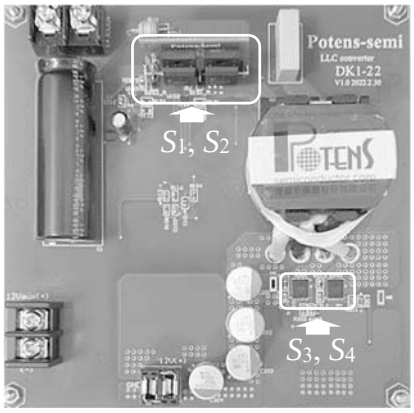

Fig. 6. The LLC circuit evaluation board.

Table 1. Parameters of main circuit.

Parameter	Value	Description
C_1	220 μF	450 V electrolytic capacitor
S_1, S_2	< 600 mΩ	650V Super Junction MOSFET
T_1	L_m=600 μH, L_r=100 μH	CC33, N_p:N_{s1}: N_{s2} = 34:2:2
C_r	68 nF	1 kV film capacitor
S_3, S_4	< 20 mΩ	65 V MOSFET
C_o	1500 μF × 4	16 V electrolytic capacitor

To compare more example, we take four different Super Junction MOSFETs for negative voltage analysis of S_1/S_2 pair [17 - 20]. Fig. 7 - 10 are the reverse current waveforms of PJF20N65N, PJF14N65N, PJF11N65N and PJF08N65N, which are measured by the reverse recovery tester. Then the measured data (the maximum reverse current of body diode, the period of the negative induced voltage, the reverse recovery charge, the reverse recovery time) and the calculation data (the negative voltage, the negative energy and the ratio of the reverse recovery charge and the reverse recovery time) are shown in Table 2 and the parasitic inductance is measured and it is about 5 nH. Table 2 shows that the negative voltage energy is proportional to the ratio of the reverse recovery charge and the reverse recovery time. It means the negative voltage energy in MOSFET application can be judged by the ratio of the reverse recovery charge and the reverse recovery time directly while choosing a new MOSFET. Fig. 11- 14 are the negative voltage of V_{GS} waveforms of PJF20N65N, PJF14N65N, PJF11N65N and PJF08N65N. These figures show that the period of the negative induced voltage and the negative voltage are close to the calculated data in Table 2. The comparison of calculated and measured negative voltage is shown in Table 3. There is above 85 % accuracy for the calculated data from the negative voltage analysis model.

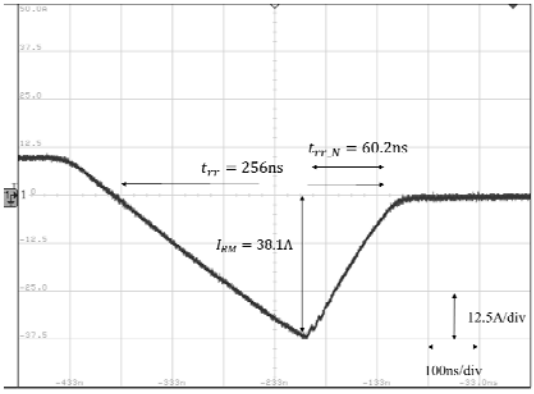

Fig. 7. The reverse current of PJF20N65N.

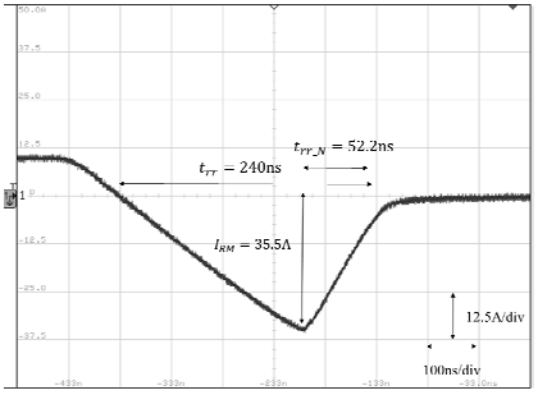

Fig. 8. The reverse current of PJF14N65N.

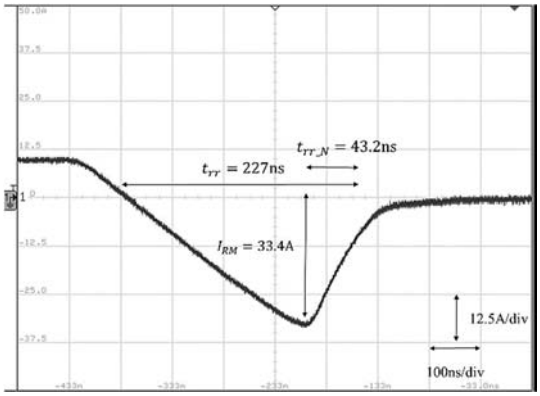

Fig. 9. The reverse current of PJF11N65N.

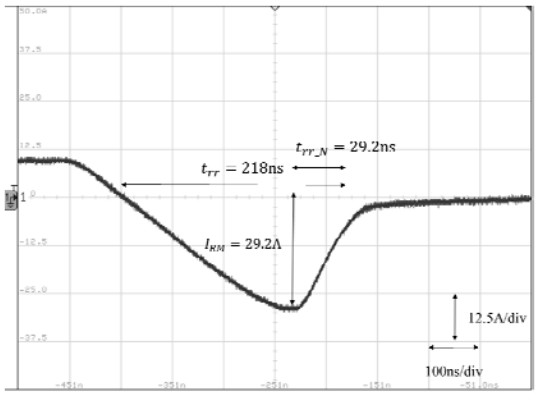

Fig. 10. The reverse current of PJF08N65N.

Table 2. MOSFET parameters and calculated negative voltage.

Part No.	t_{rr} (ns)	Q_{rr} (nC)	I_{RM} (A)	t_{rr_N} (nS)	V_{LP1} (V)	A (V·ns)	$\frac{Q_{rr}}{t_{rr}}$
PJF20N65N	256	5233	38.1	60.2	-3.2	193	20.4
PJF14N65N	240	4576	35.5	52.2	-3.4	177	19.1
PJF11N65N	227	4025	33.4	43.2	-3.85	168	17.7
PJF08N65N	218	3888	29.2	42.7	-3.4	145	15.5

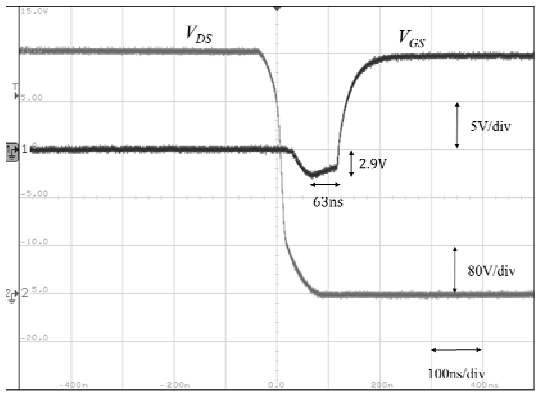

Fig. 11. The negative voltage of PJF20N65N.

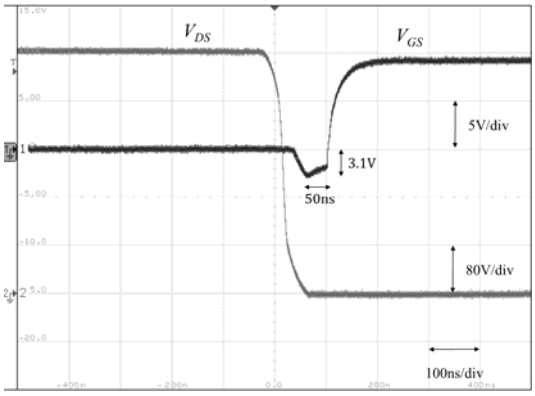

Fig. 12. The negative voltage of PJF14N65N.

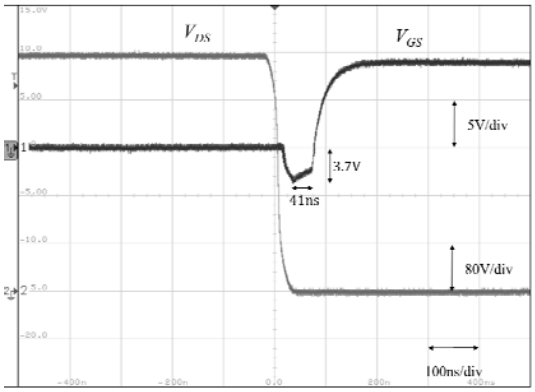

Fig. 13. The negative voltage of PJF11N65N.

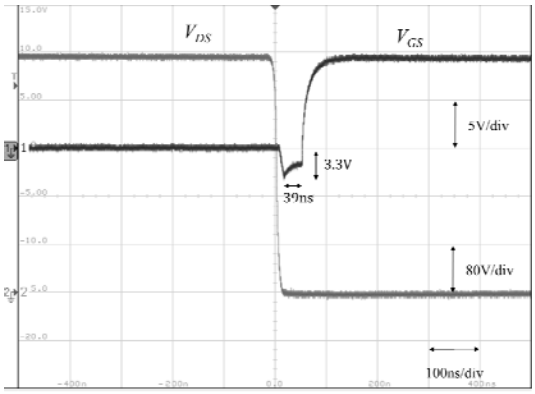

Fig. 14. The negative voltage of PJF08N65N.

Table 3. Calculated and measured negative voltage.

Part No.	Calculated data		Measured data		Error	
	V_{LP1} (V)	A (V·ns)	V_{LP1} (V)	A (V·ns)	V_{LP1} (%)	A (%)
PJF20N65N	-3.2	193	2.9	183	10.3%	5.5%
PJF14N65N	-3.4	177	3.1	155	9.7%	14.2%
PJF11N65N	-3.85	168	3.7	152	5.4%	10.5%
PJF08N65N	-3.4	145	3.3	129	3.0%	12.4%

For synchronous rectifier, we also take four different low voltage MOSFETs for negative voltage and R_g impact analysis of S_2/S_4 pair [21 - 24]. Fig. 15 shows the turn on waveforms of the PDEC69F0BX-5 which R_g is 26 Ω, and Fig. 16 shows the turn on waveforms of the PDC6974X-5 which R_g is 1.8 Ω. Fig. 17 shows the turn on waveforms of the PDC6986BX-5 which R_g is 0.9 Ω. Fig. 18 shows the turn on waveforms of the PDC6988X-5 which R_g is 0.3 Ω. These results shows that a larger R_g will have a smaller negative voltage. From above analysis, we could also conclude that the large ratio of the reverse recovery charge and the reverse recovery time is the highest possibility to damage the gate drive pin of the control IC.

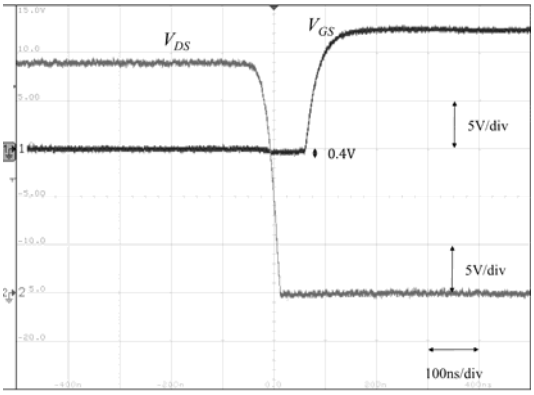

Fig. 15. The negative voltage of PDEC69F0BX-5.

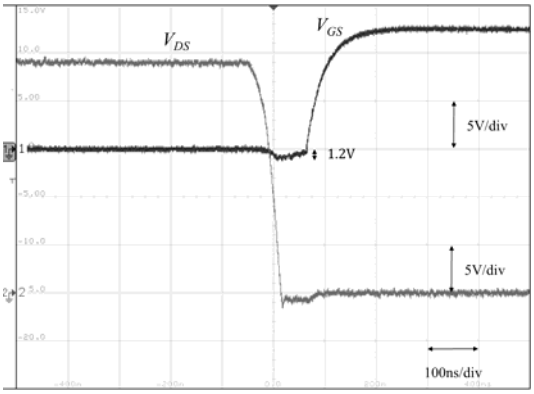

Fig. 16. The negative voltage of PDC6974X-5.

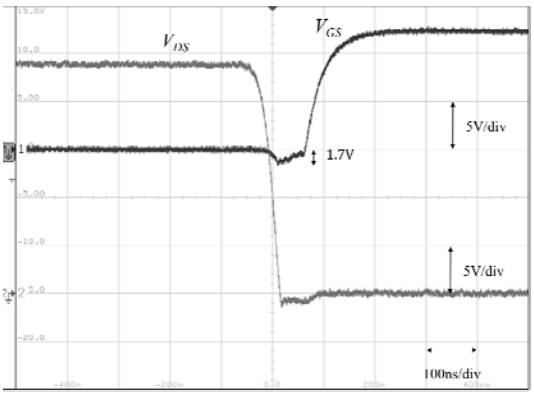

Fig. 17. The negative voltage of PDC6986BX-5.

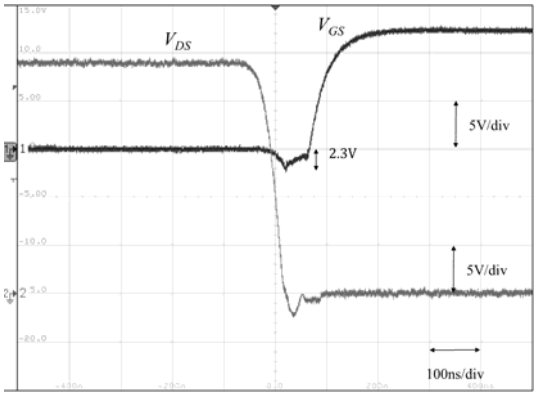

Fig. 18. The negative voltage of PDC6988X-5.

4. Conclusions

This paper shows an analysis method to evaluate the influence of the negative voltage caused by the parasitic inductance of the MOSFET lead and PCB circuit trace and an impact on the drive pin of the control IC. The reverse recovery time is also the highest possibility to damage the gate drive pin of the control IC. The more duration the negative voltage sustains, the more possibility that the control IC will be damaged. However, we could reduce the negative voltage drop at the gate drive pin by increasing the gate drive resistor to avoid IC damaged.

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